US009483405B2

(12) **United States Patent**
Miura et al.

(10) **Patent No.: US 9,483,405 B2**
(45) **Date of Patent: Nov. 1, 2016**

(54) **SIMPLIFIED RUN-TIME PROGRAM TRANSLATION FOR EMULATING COMPLEX PROCESSOR PIPELINES**

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(*) Notice: Subject to any disclaimer, the term of this patent is extended or adjusted under 35 U.S.C. 154(b) by 1560 days.

(21) Appl. No.: **12/234,671**

(22) Filed: **Sep. 21, 2008**

(65) **Prior Publication Data**

US 2009/0083513 A1 Mar. 26, 2009

Related U.S. Application Data

(60) Provisional application No. 60/973,994, filed on Sep. 20, 2007.

(51) **Int. Cl.**
G06F 12/02 (2006.01)
G06F 12/08 (2016.01)
G06F 12/10 (2016.01)

(52) **U.S. Cl.**
CPC ***G06F 12/0855*** (2013.01); ***G06F 12/1009*** (2013.01)

(58) **Field of Classification Search**
None
See application file for complete search history.

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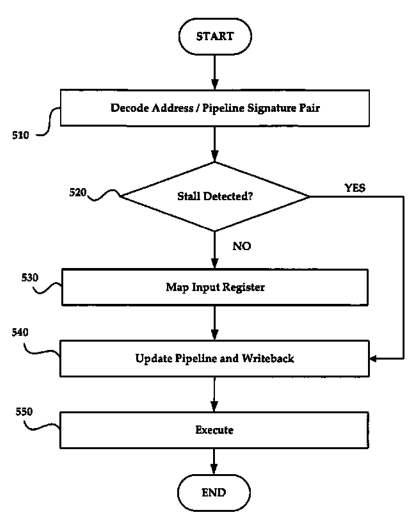
(57) **ABSTRACT**

Simplification of run-time program translation for emulating complex processor pipelines is disclosed. Dynamic pipeline states are moved into a cache lookup process leaving a code translation process to deal only with static pipeline states. With dynamic pipeline states removed from the translation process, translation becomes more simple and efficient like that of a non-pipelined processor.

16 Claims, 6 Drawing Sheets



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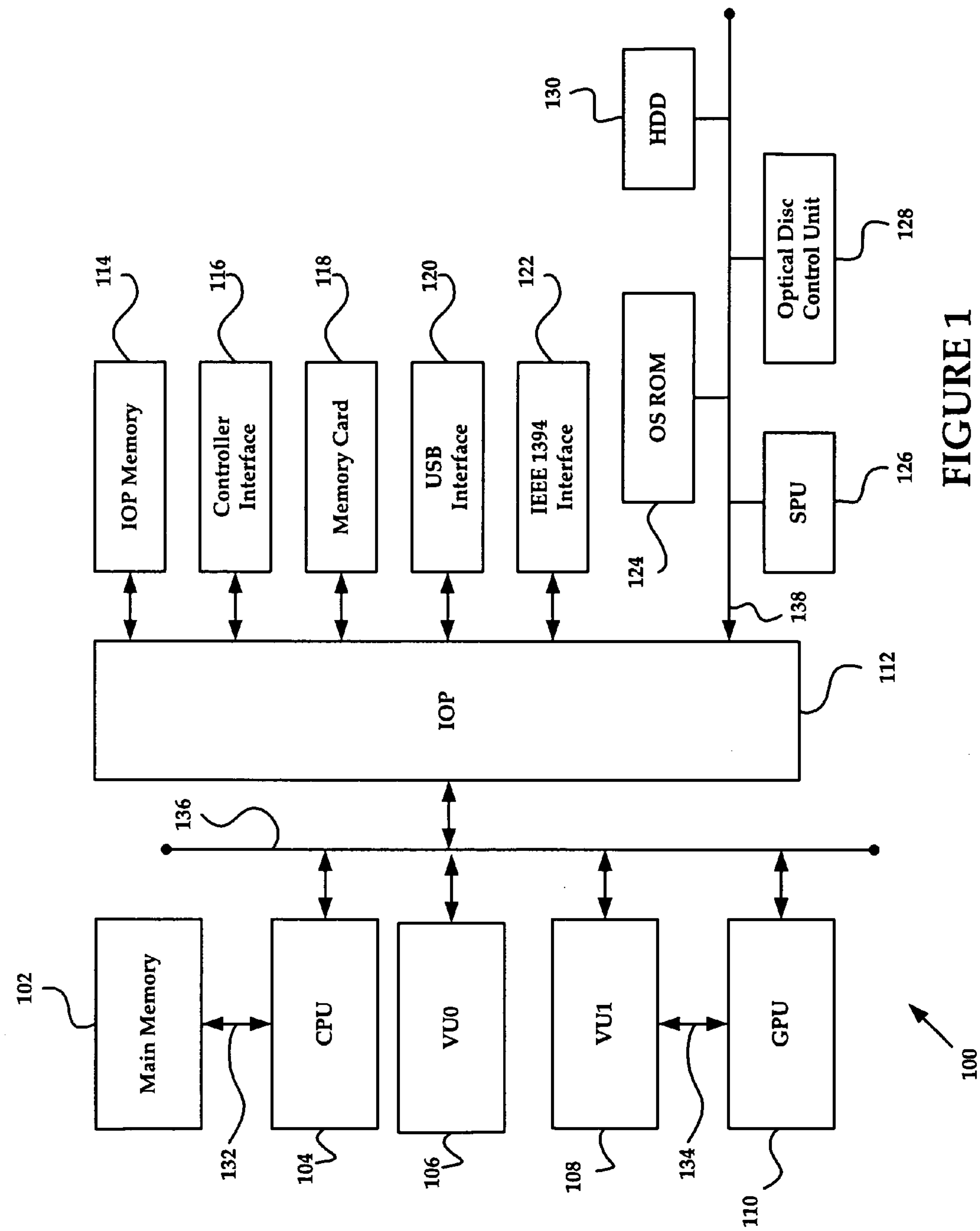
Main Memory
CPU
VU0
VU1
GPU
IOP
IOP Memory
Controller Interface
Memory Card
USB Interface
IEEE 1394 Interface
OS ROM
HDD
SPU
Optical Disc Control Unit
100
102
104
106
108
110
112
114
116
118
120
122
124
126
128
130
132
134
136
138

FIGURE 1

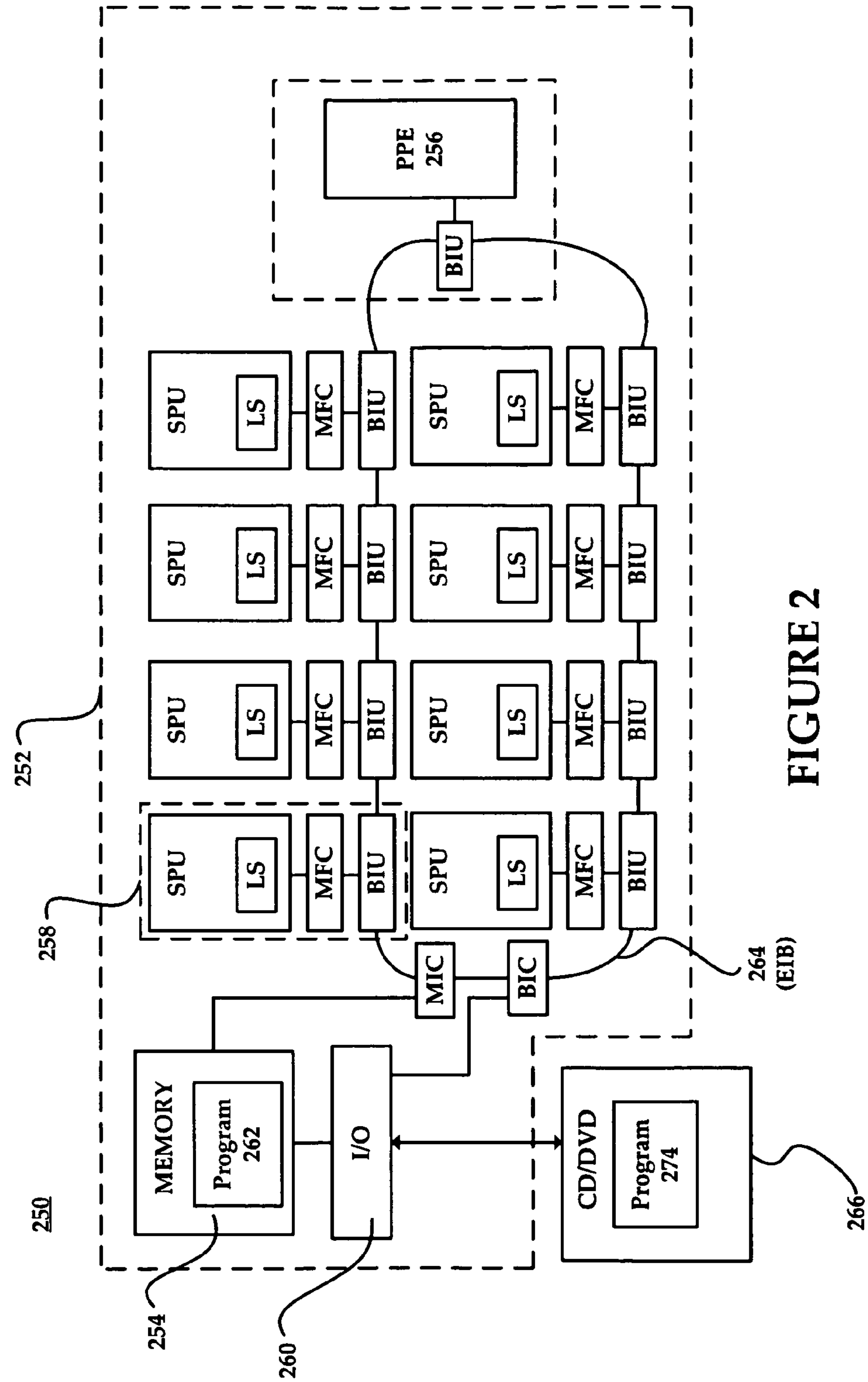
250
252
258
PPE
256
BIU
SPU
LS
MFC
MIC
BIC
264
(EIB)
MEMORY
Program
262
I/O
CD/DVD
Program
274
254
260
266

FIGURE 2

CACHE ENTRY	KEY ADDRESS	TRANSLATION ADDRESS
# 1	Target 0x1000	Host 0x2000
# 2	Target 0x1010	Host 0x2040
# 3	Target 0x1020	Host 0x2100
. . .	. . .	. . .

FIGURE 3

CACHE ENTRY	KEY ADDRESS	PIPELINE SIGNATURE	TRANSLATION ADDRESS
# 1.0	Target 0x1000	A	Host 0x2000
# 1.1	_*_	B	Host 0x2040
# 2.0	Target 0x1010	C	Host 0x2060
# 2.1	_*_	D	Host 0x2090
# 2.2	_*_	E	Host 0x2100
# 3.0	Target 0x1020	F	Host 0x2230
...	...	...	...

FIGURE 4

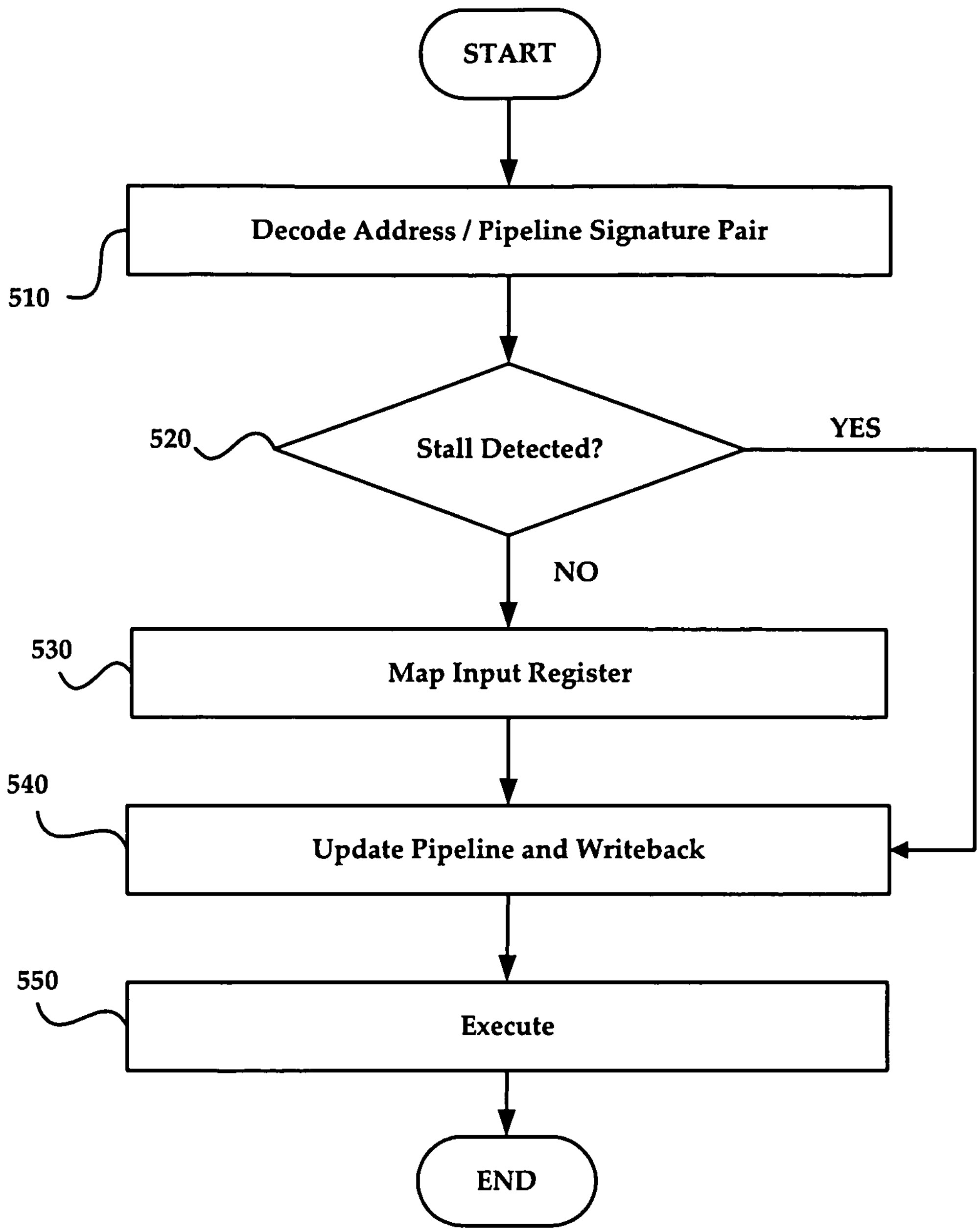
START
Decode Address / Pipeline Signature Pair
510
Stall Detected?
520
YES
NO
Map Input Register
530
Update Pipeline and Writeback
540
Execute
550
END

FIGURE 5

PPU REGISTER	EMULATED REGISTER
GPR0	VID[0]
GPR1	VID[1]
GPR2	VID[2]
GPR3	VID[3]
VPR0	MAC[0]
VPR1	MAC[1]
VPR2	MAC[2]
VPR3	MAC[3]
VPR4	CLIP[0]
VPR5	CLIP[1]
VPR6	CLIP[2]
VPR7	CLIP[3]
VPR8	NextQ

FIGURE 6

SIMPLIFIED RUN-TIME PROGRAM TRANSLATION FOR EMULATING COMPLEX PROCESSOR PIPELINES

CROSS-REFERENCE TO RELATED APPLICATIONS

The present application claims the priority benefit of U.S. provisional patent application No. 60/973,994 filed Sep. 20, 2007 and entitled "Simplified Run-Time Program Translation for Emulating Complex Processor Pipelines," the disclosure of which is incorporated herein by reference.

This application is related to Patent Cooperation Treaty application number PCT/GB2007/000587 filed Feb. 19, 2007 in the name of Sony Computer Entertainment Inc., the disclosure of which is incorporated herein by reference.

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention generally relates to complex processor pipelines. More specifically, the present invention relates to microcode implementation of run-time program translation for emulating said pipelines.

2. Description of the Related Art

A processor pipeline is a whole processing task or workload broken into smaller sub-tasks. Through the use of processor pipelining, instruction throughput (i.e., the number of instructions that can be executed in a unit of time) can be increased. Each sub-step of the overall task carries data at once and each sub-step is connected to a subsequent sub-step effectively creating links in a pipe.

In an elementary form, the processing of a computer instruction is split into a series of independent steps with a storage operation at the conclusion of each step. This allows control circuitry of a computing device to issue instructions at the processing rate of the slowest step. Even at the rate of the slowest step, the overall processing is still faster than the time required to perform all of the steps constituting the whole instruction at once. Pipelining in this manner allows multiple tasks to be executed in parallel. As a result, central processing units (CPU) and/or other logic units are kept as busy as possible as often as possible.

In this context, an ideal pipeline could be conceived with (for example) 50-stages and a 50 GHz clock rate that would allow for processing tasks at 50 billion times per second. Reality would dictate otherwise with respect to pipeline depth, however, as the code running in a processor must be programmed without margins for error or guesswork. The near constant calling of sub-routines or functions runs the risk of guessing a wrong branch thereby invalidating the incorrectly guessed workload, which would require the pipeline to refill completely thereby reducing performance. The possibility for increases with the number of pipeline stages.

It is, therefore, the nature of a complex pipelined processor that code execution is affected by current pipeline state. The pipeline state is dynamic and affected by previously executed code. In translating code for a complex pipelined processor, the rules of the pipeline must be followed to produce a correct translation.

The prior art has generally relied on one of two options to address the aforementioned constraints of complex pipelined processors, neither of which have resulted in significant success. The first option is to completely emulate the processor pipeline at all times. The second option is to use what is commonly referred to as a global analysis approach for an entire program to evaluate the dynamics of the program.

While the first solution is relatively simple, it generally results in reduced performance. The latter solution has the potential to increase performance of translated code but does so in the context of high implementation complexity and high translation cost. The global analysis method, too, may not be able to handle all cases and full pipeline emulation may be required as a fallback.

There is, therefore, a need in the art to simplify the microcode implementation of run-time program translation for emulating complex processor pipelines.

SUMMARY OF THE INVENTION

Embodiments of the present invention simplify the microcode implementation of run-time program translation for emulating complex processor pipelines. The disclosed embodiments offer the benefits of simple implementation, high performance, and applicability to a wide array of pipelining problems.

In a first claimed embodiment, a method for program translation in a processor pipeline is disclosed. Through this method, a current target address and pipeline signature are determined. A corresponding target address and pipeline signature entry are looked up. A translation is produced for the current target address and pipeline signature when there is no corresponding target address and pipeline signature entry.

A second claimed embodiment also provides for a method of program translation in a processor pipeline. A current target address and pipeline signature are determined. A corresponding target address and pipeline signature entry are looked up and a translation corresponding to the target address and pipeline signature are executed. This execution occurs when a corresponding target address and pipeline signature entry are available.

A third claimed embodiment recites a processor pipeline translation method. Through this method, an address pipeline signature pair is decoded and checked for a stall. A code generation function for lower and upper instructions is called and the address pipeline pair is updated.

BRIEF DESCRIPTION OF THE DRAWINGS

FIG. **1** is an illustration of an exemplary computing system, specifically that of the PlayStation®2 from Sony Computer Entertainment Inc.

FIG. **2** is an illustration of an alternative exemplary computing system, specifically that of the PlayStation®3 from Sony Computer Entertainment Inc.

FIG. **3** illustrates an exemplary translation cache structure including a cache entry, key address, and translation address.

FIG. **4** illustrates an exemplary translation cache structure including a cache entry, key address, pipeline signature, and translation address.

FIG. **5** illustrates an exemplary translation process as may be executed in an embodiment of the present invention.

FIG. **6** illustrates an exemplary register mapping on entry to a translated block as may occur in an embodiment of the present invention.

DETAILED DESCRIPTION

In an exemplary embodiment of the present invention, a translator statically translates a single Vector Processing

Unit (VU) basic block at a time from a given Entry PC until a branch instruction—[M] bit—or end of program—[E] bit. With respect to statistical translation, each translation is based on a single VU pipeline state at the entry point. The initial pipeline state is statically driven forward one cycle at a time. Code is emitted for each instruction and the final VU pipeline state is recorded. Pipelines are not driven at runtime because the pipeline state is always known at compile time.

A pipeline state may be referred to as a pipeline signature. Translations may be saved in a cache that can be looked up by pair of entry program counter addresses of translated code blocks and a corresponding pipeline signature. This information may be representative of certain snapshots of the processor's pipeline state.

A translation cache is used to hold translated code so that that the code does not have to be re-translated repeatedly. An ordinary translation cache may normally be keyed using the program counter address of translated code blocks. The present invention adds an additional key—the aforementioned pipeline signature. This signature allows one program address to correspond to multiple cached translations, each one keyed by a different pipeline signature.

Through the present invention, the problem of the dynamic pipeline state is effectively moved into the cache lookup process and leaves the code translation process to deal only with static pipeline states. With dynamic pipeline state removed from the translation process, translation becomes as simple and efficient as that for a non-pipelined processor. This method may also have applications in microprocessor design where modern processors often involve code translation form a higher-level instruction code into microcode.

Embodiments of the present invention may be implemented in the context of emulating the VU of the PlayStation®2 (as referenced with respect to FIG. **1**) on another computing device such as the PlayStation®3 (as reference with respect to FIG. **2**), which may not necessarily utilize the aforementioned VU. The emulation techniques referenced herein are taught in the context of a PlayStation®2 entertainment system. Notwithstanding, these techniques may be implemented in other computing environments. In this regard, any reference to emulating the VU of the PlayStation®2 vis-à-vis the PlayStation®3 or any other computing device is exemplary and solely for the purpose of illustration.

FIG. **1** is an illustration of an exemplary computing system **100**, specifically that of the PlayStation®2 from Sony Computer Entertainment Inc. The elements identified in FIG. **1** are exemplary and may include various alternatives, equivalents, or derivations thereof. The system **100** may include, but is not limited to, a main memory **102**, a central processing unit (CPU) **104**, vector processing units VU**0** **106** and VU**1** **108**, a graphics processing unit (GPU) **110**, all of which may be coupled via a bus **136** to an input/output processor (IOP) **112**. The system **100** may also include an IOP memory **114**, a controller interface **116**, a memory card **118**, a Universal Serial Bus (USB) interface **120**, and an IEEE 1394 interface **122**. The system **100** may further include an operating system read-only memory (OS ROM) **124**, a sound processing unit (SPU) **126**, an optical disc control unit **128**, and a hard disc drive (HDD) **130**, all of which may be connected via a bus **138** to IOP **112**.

The CPU **104**, the VU**0** **106**, the VU**1** **108**, the GPU **110**, and the IOP **112** may communicate via a system bus **132**. The CPU **104** may communicate with the main memory **102** via a dedicated bus **134**. The VU**1** **108** and the GPU **110** may also communicate with one another via a dedicated bus **134**. The CPU **104** executes programs stored in the OS ROM **124** and the main memory **102**. The main memory **102** may contain pre-stored programs and may also contain programs transferred via the IOP **112** from a CD-ROM, DVD-ROM, or other optical disc (not shown) using the optical disc control unit **128**. The IOP **112** may be configured to control data exchanges between the CPU **104**, the VU**0** **106**, the VU**1** **108**, the GPU **110** and other devices of the system **100**, such as the controller interface **116**, or from other such systems via a network adaptor (not shown).

The GPU **110** may execute drawing instructions from the CPU **104** and the VU**0** **106** to produce images for display on a display device (not shown). The VU**1** **108** may be configured to transform objects from three-dimensional coordinates to two-dimensional coordinates, and send the two-dimensional coordinates to the GPU **110**. The SPU **126** may execute instructions and processes data to produce sound signals that are output on an audio device (not shown).

A user of the system **100** may provide instructions via the controller interface **116** to the CPU **104**, which may be coupled to a control device including the likes of a joystick, directional buttons, and/or other control buttons. For example, the user may instruct the CPU **104** to store certain game information on the memory card **118**, which may be removable (e.g., a flash memory or other non-volatile memory card), or may instruct a character in a game to perform some specified action. Other devices may be connected to the system **100** via the USB interface **120** and/or the IEEE 1394 interface **122**.

The system **100** is, in one embodiment, an electronic gaming console; however, the system **100** (or portions thereof) may also be implemented as a general-purpose computer, a set-top box, a hand-held gaming device, or in a mobile device such as a cellular phone. It should further be noted that various other system architectures may be utilized within the scope of the present invention.

FIG. **2** is an illustration of an alternative exemplary computing system, specifically that of the PlayStation®3 from Sony Computer Entertainment Inc. The PlayStation® (3) of FIG. **2** (i.e., the electronic entertainment system **250**) is based on use of a Cell processor **252**. The elements identified in FIG. **2** are exemplary and may include various alternatives, equivalents, or derivations thereof. Certain aspects of a computer architecture and high speed processing model utilizing a Cell processor are disclosed in U.S. patent publication number 2002-0138637 for a "Computer Architecture and Software Cells for Broadband Networks," the disclosure of which is incorporated herein by reference. The Cell processor architecture represents the work of Sony Computer Entertainment Inc., Kabushiki Kaisha Toshiba, and International Business Machines Corporation.

Through the use of the aforementioned Cell processor, data and applications may be processed and packaged into uniquely identified and uniformly formatted software cells. The uniformity of structure and unique identification facilitates the processing of applications and data throughout a network of Cell processor equipped computing devices. For example, one computing device may formulate a software cell but can distribute that cell to another device for processing. Thus, the cells may migrate throughout a network for processing on the basis of the availability of processing resources on the network.

The cell processor **252** of FIG. **2** includes a main memory **254**, a single power processor element (PPE) **256**, and eight synergistic processor elements (SPE) **258**. The cell processor **252** may be configured, however, with more than one

PPE and any number of SPEs **258**. Each SPE **258** of FIG. **2** includes a synergistic processor unit (SPU) and a local store (LS).

Main memory **254**, PPE **256**, and SPEs **258** may communicate with each other and with an I/O device **260** over, for example, a ring-type-element interconnect bus (EIB) **264** coupled to a bus interface controller (BIC). The PPE **256** and SPEs **258** may access the EIB **264** through bus interface units (BIU). The PPE **256** and SPEs **258** may access the main memory **254** over the EIB **264** through memory flow controllers (MFC) and memory interface controller (MIC).

Main memory **254** may include a program **262** that implements executable instructions. The instructions may be read from a CD/ROM or other optical disc in CD/DVD reader **266** coupled to the I/O device **260**, the CD/ROM or other optical disc being loaded into the reader **266**. The CD/ROM, too, may comprise a program, executable instructions, or other data **274**.

In some embodiments, PPE **256** may be a standard processor capable of stand-alone processing of data and applications. In operation, PPE **256** may schedule and orchestrate the processing of data and applications by SPEs **258** and the associated SPU. In one embodiment, the SPU may be a single instruction, multiple data (SIMD) processor. Under the control of PPE **256**, the SPUs may process data and applications in a parallel and independent manner. MIC may control accesses by PPE **256** SPUs to data and applications in main memory **254**.

Returning to FIG. **1**, an exemplary VU may include thirty-two 128-bit registers, sixteen 16-bit fixed point registers, four floating-point multiply accumulate (FMAC) units, a floating point divide (FDIV) unit and a local data memory. In the case of the PlayStation® 2 of FIG. **1**, which includes two VUs, the data memory for a first VU may be 4 KiB in size while the second VU may features a 16 KiB data memory. To achieve high bandwidth, the VU's data memory may be connected directly to a graphics interface (GIF) and both of the data memories can be read directly by, for example, a ten-channel director memory access (DMA) unit.

A single vector instruction may consist of four 32 bit IEEE compliant single precision floating point values, which may be distributed to the four single precision (32 bit) FMAC units for processing. The FMAC units may have an instruction latency of four cycles but a six stage pipeline allowing for a throughput of one cycle per an instruction. The FDIV unit may have a nine stage pipeline and may be configured to execute one instruction every seven cycles.

The VU, in an embodiment, is a Very Long Instruction Word (VLIW) pipelined execution processor. Because the VU is a VLIW complexly pipelined execution processor, a series of problems are presented that may require cycle-accurate pipeline emulation: (1) instruction sets with various different latencies; (2) a mixture of hazard checking as some instructions are hazard checked and some are not, which imposes the requirement of correct cycle-accurate emulation; (3) register forwarding exceptions where, under certain circumstances, input arithmetic logic unit (IALU) registers are forwarded in different ways and which may require emulating a 5-cycle deep pipeline in order to emulate IALU registers correctly; and (4) as the VU executes two instruction pipes in parallel, certain conflicts between the two pipes may arise and that alter execution behavior.

A partial list of pipeline issues that require special attention on a VU include: (1) hazard checking on vector floating point (VFP) registers as instructions may stall based on previously executed instructions; (2) a Q pipeline stall if multiple Q instructions are issued; (3) a P pipeline stall if multiple P instructions are issued as non-hazard-checked Q & P registers require delayed register updates; (4) non-hazard checked MAC & CLIP registers, which require delayed register updates; and (5) VI register forwarding to the branch pipeline requires emulating IALU write back for 5 pipeline cycles.

As noted previously, code translation for such a complex system can be approached in one of two ways: a local translation approach and a global translation approach. A local translation approach involves translating only independent, relatively small blocks of code in isolation of the rest of the program, using a Just-in-Time (JIT) requirement system. As blocks are translated in isolation, the translation must account for any possible pipeline states. As such this kind of translation requires emulating the CPU pipeline at runtime at all points in the translated code. For a processor as complex as the VU of FIG. **1**, the overhead of pipeline emulation may very high and dwarf the rest of the system.

A global translation approach involves analyzing a whole program. Analysis of data-flow and pipeline states throughout a whole program can result in optimizations whereby the pipeline need not be fully emulated all of the time. This can yield much better performance than the local translation approach at the cost of a much greater degree of implementation complexity. Further, this method has a high translation time cost, has non-linear complexity, and as such has application only to small programs, and does not always yield optimal results.

Turning now to a local translation method that overcomes some of the drawbacks of the previously implemented local and global approaches, it is noted that the processor pipeline state may change at any point in program execution based on previously executed instructions. A pipeline signature is a compact way to represent the current state of VU**0** pipelines—a snapshot of the pipeline state. The state of the pipeline is incorporated in the pipeline signature in a compact manner; for example, the current stage number of a pipeline, which registers cause hazards or at what cycle will a certain register value update.

For a complex CPU such as the VU of the PlayStation®2, sufficient information could be captured within a 128-bit pipeline signature. From this signature, the complete pipeline state may be deduced. The pipeline signature contains sufficient information to be able to resume correct VU**0** pipeline execution at any time and to facilitate efficient translation.

The signature helps keep the translator simple while supporting all the complexity of VU**0** pipelines efficiently. The pipeline signature may be made up of the following elements and, by these definitions, a pipeline signature may (and in some cases shall) occupy less than 128 bits:

Q Pipeline State (QPS) 4 bits: a Q pipeline is either idle or executing for a maximum of 13 cycles thus Q Pipeline State saves a 4 bit value for 0 to 13 cycles.

VPU Float Register History (VFR[3] [2]) 54 bits: up to two VF registers may be modified in each cycle (one by lower and one by upper pipeline). Each VF register is uniquely identified by 9 bits (5 bits for register number 0 to 31 and 4 bits mask for XYZW fields). VU pipeline may be stalled by VF register history from the past 3 cycles thus VF Register History saves 3 cycles*2 registers*9 bits.

VPU Integer Register History (VIR[4]) 16 bits and (VIS [4]) 4 bits: up to one VI register may be modified in each cycle (by lower pipeline). Each VI register is uniquely identified by 4 bits (register number 0 to 15). VU pipeline may be stalled by VI register history for the past 3 cycles. It is also necessary to cope with IALU→BRANCH hazard, which is partly addressed by keeping the register history for 4 cycles whereby VIRD saves 4 cycles*1 register*4 bits. VISD, is an extra 1 bit associated with each VIR[ ] value above that indicates if reading the VIR register causes stalls.

IALU History (IALUH) 1 bit: A 1 bit flag indicates if the last cycle executed was an IALU instruction (for IALU→BRANCH hazard).

Branch History (BH) 1 bit: A 1 bit flag indicates if the last instruction executed was a taken BRANCH (for branch-in-branch handling).

E-bit History (EH) 1 bit: A 1 bit flag indicates if E-bit was set on the last instruction (for end of program handling).

Extra Information to Aid Efficient Translation 32 bits: In one embodiment, 6 bits may be dedicated to help optimize the MAC Flag pipeline status, 6 bits to help optimize the CLIP Flag pipeline status, and 4*5 bits to help optimize the integer pipeline status.

FIG. **3** illustrates an exemplary translation cache structure including a cache entry, key address, and translation address. Normally a translation cache may be used to cache code translations. Previous translations can be looked up in the cache using a key. Generally the key may be the target program counter address, and the value may be the translation's host address as in FIG. **3**. Had the target address 0x1010 been required, for example, a match would occur to translation entry #**2**, which would yield host address 0x2040. This system allows a one-to-one mapping of target address to host translation address.

FIG. **4** illustrates an exemplary translation cache structure including a cache entry, key address, pipeline signature, and translation address. In a Pipeline Signature cache the key is built up of both the target address and a Pipeline Signature as in FIG. **4**. Had the target address 0x1001 together with Pipeline Signature 'D' been required, for example, a match would occur to translation entry #**2.1** which would yield host address 0x2090. This system allows multiple entries in the cache for each target address.

With the Pipeline Signature incorporated in the cache lookup process, simplification of the translation process is possible. In FIG. **3**, translation #**2** must correspond to any potential pipeline state, in other words the pipeline state is dynamic on entry to translation #**2** within this translation and must be translated as such. In FIG. **4**, translation #**2.1** corresponds to a single pipeline signature, and as such to a single pipeline state. With the pipeline state now static, translation #**2.1** can be generated and optimized specifically for that single pipeline state. With the pipeline being static, the translation process is simplified and can handle all pipelining attributes, has linear complexity, and can be optimized to do a minimal amount of processing given the fixed pipeline conditions.

FIG. **5** illustrates an exemplary translation process as may be executed in an embodiment of the present invention. At any point in translating or executing the target program, the current target address and pipeline signature is known. Cache entries for a corresponding target address and pipeline signature entry are looked up. This process can be most efficient if the entries are stored in a hash table.

If there is no match, a translation is produced for the current target address and pipeline signature. These are static values and the translation is valid only for the address and pipeline signature pair. This translation is saved in the translation cache and may be subsequently executed. If there is a match, this translation is likewise executed.

Wherever there are static branches in translated code, new target address and Pipeline Signature for the branch target is known statically at translation time. Since this is static a cache lookup, it need not be done at run-time. A one off lookup is needed at translation time. Whenever there are dynamic branches in translated code a cache lookup must be done at run-time. Translation at each cycle may be divided into the following steps.

Step **510** may be characterized as a decoding translation stage. At this stage, the current address pipeline signature pair is decoded, which prepares information about the instructions for step **520** and **530**.

In step **520**, which may be characterized as a stall determination stage, VF and VI stalls are checked using current VFRD, VIRU, and VIS[ ] information. If a stall is detected, translation skips to translation step **540**.

In step **530**—the register mapping and instruction generation stage—the code generation function gen_func is called for the lower and upper instructions. Control flow, next program counter and program termination may also be determined at this stage. Each gen_func maps the input registers it requires and emits computation. The result may not be conceptually written back to the register file at this time but may be kept in a temporary register and a record may be made for the write back phase. This avoids write back hazards when Upper & Lower pipe modify and/or read the same register on the same cycle.

For example, a first write back hazard may include the upper and lower pipes writing the same VF register. In response, the following is proposed: add vf01, vf00, vf00??? Iq vf01,)(vi00). A second such hazard might be the upper pipe reading the VF register that is modified by the lower pipe. In response, the following is proposed: add vf02, vf01, vf00??? Iq vf01, 0(vi00).

In some embodiments, only the lower pipe VF register write may need to be delayed to get around the write back hazards. The upper pipe may go direct to the real VF register. The lower pipe VF results may be kept in a temporary register and then re-mapped to a real VF register at step **540**.

In step **540**—the pipeline update and write back stage—the pipeline update and write back involves the following. First, write back VIR[0] & VID[0] to VI register file, which may be done through register re-naming. Second, write back VF registers recorded during step **530**, which may be done by registered renaming in observance of a write back hazard where the upper and lower pipes writing the same VF register. Thirdly, update the MAC and CLIP flags pipeline, which may be done through register re-naming. The pipeline signature update is then complete, and translation is executed at step **550**.

With respect to the aforementioned register re-naming, emulated registers may be assigned to real PPU registers during translation. Re-naming means re-assigning real PPU registers from one emulated register to another. No actual move instructions are involved. For example, VID[0] is currently stored in PPC GPR $r1. $r1 is named VID[0]. VID[1] is currently stored in PPC GPR $r2. $r2 is named VID[1]. Renaming $r2 to VID[0] is equivalent to the operation VID[0]=VID[1].

The Pipeline Signature is conceptually updated at each cycle during translation as follows using register re-naming. For example:

VIR[0]=VIR[1]; VID[0]=VID[1]; VIS[0]=VIS[1];
VIR[1]=VIR[2]; VID[1]=VID[2]; VIS[1]=VIS[2];
VIR[2]=VIR[3]; VID[2]=VID[3]; VIS[2]=VIS[3];
VIR[3]=New VI Register; VID[3]=New VI Data;
VIS[3]=1 if ILW* instruction executed, else 0;
IALUH=1 if IALU instruction executed, else 0;
BH=1 if taken BRANCH executed, else 0;

EH=1 if E-bit executed, else 0;

QPS decrements to zero; When QPS=0 the Q register updates.

With respect to VF register mapping, VF registers are not delayed, thus they are mapped direct from the VF register file.

Concerning VI Register Mapping and IALU→BRANCH Hazard, VI registers are delayed 4 cycles in VID[ ]. In some instances, if a VI register hits a VID, it is mapped direct to that VID (i.e., VID Forwarding). If a VI register misses VID it is mapped direct from the VI register file. When IALU→BRANCH hazard is detected, VID Forwarding is skipped. IALU→BRANCH hazard is detected using IALUH and VIR[0] as follows:

```
II For VI register N
   if(IALUH=1 && N=VIR[0])
   Read N direct from register file VI[N]
   else
   Register N is forwarded from VID[ ]
```

FIG. **6** illustrates an exemplary register mapping on entry to a translated block as may occur in an embodiment of the present invention. The initial register mapping must be fixed because it is not saved in the pipeline signature. Depending upon space available in the pipeline signature, these could also be saved and then they would not have to be fixed.

Computer-readable storage media refer may be utilized to provide instructions to a processor for execution, including instructions that correspond to the methodology of FIG. **3**. Various forms of transmission media may be involved in carrying one or more sequences of one or more instructions to a processor for execution.

While various embodiments have been described above, it should be understood that they have been presented by way of example only, and not limitation. The descriptions are not intended to limit the scope of the invention to the particular forms set forth herein. Thus, the breadth and scope of a preferred embodiment should not be limited by any of the above-described exemplary embodiments. It should be understood that the above description is illustrative and not restrictive.

Further, the present descriptions are intended to cover such alternatives, modifications, and equivalents as may be included within the spirit and scope of the invention as defined by the appended claims and otherwise appreciated by one of ordinary skill in the art. The scope of the invention should, therefore, be determined not with reference to the above description, but instead should be determined with reference to the appended claims along with their full scope of equivalents.

What is claimed is:

1. A method for program translation in a processor pipeline, the method comprising:

determining a current target address and pipeline signature, the pipeline signature including a state of the processor pipeline, the pipeline signature allowing one program address to correspond to multiple cached translations, each cached translation keyed by a different pipeline signature;

requesting a translation based at least in part on the current target address and the pipeline signature, the translation including instructions translated for a processor; and

generating the translation when the translation is unavailable, the translation valid for only a single address and pipeline signature pair.

2. The method of claim **1**, wherein the target address and pipeline signature are looked up in a hash table.

3. The method of claim **1**, wherein the target address and pipeline signature are static values.

4. The method of claim **1**, further comprising saving the translation in a translation cache.

5. The method of claim **4**, further comprising executing the translation.

6. The method of claim **1**, wherein the translation includes translating instructions to an instruction set of the processor.

7. A method for program translation in a processor pipeline, the method comprising:

determining a current target address and pipeline signature, the pipeline signature including a state of the processor pipeline, the pipeline signature allowing one program address to correspond to multiple cached translations, each cached translation keyed by a different pipeline signature;

requesting a translation based at least in part on the current target address and the pipeline signature, the translation including instructions translated for a processor; and

executing the translation when the translation is unavailable, the translation valid for only a single address and pipeline signature pair.

8. The method of claim **7**, wherein the target address and pipeline signature are looked up in a hash table.

9. The method of claim **7**, wherein the target address and pipeline signature are static values.

10. A processor pipeline translation method, comprising:

decoding a current target address and pipeline signature, the pipeline signature including a state of a processor pipeline, the pipeline signature allowing one program address to correspond to multiple cached translations, each cached translation keyed by a different pipeline signature;

checking for a stall;

calling a code generation function to translate instructions for a processor for lower and upper instructions; and

updating an address pipeline signature pair, for which a generated translation is valid for only the address pipeline signature pair.

11. The method of claim **10**, wherein the code generation function maps required input registers.

12. The method of claim **11**, wherein the mapped input registers are maintained in a temporary register.

13. The method of claim **12**, further comprising creating a record for a write back operation.

14. The method of claim **11**, further comprising writing back the mapped input registers to a register file.

15. The method of claim **10**, wherein the stall is checked with respect to VF and VI stalls.

16. The method of claim **15**, wherein the stall is checked using current VFRD, VIRU, and VIS[ ] information.

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